REMARKS

This response is a full and complete response to the non-final Office Action dated December 4, 2006. In the present Office Action, claims 1-16 are pending in the application, claims 1-16 stand rejected, and the drawing is objected to. The Examiner has acknowledged the claim for priority. The Examiner has also noted that consideration has been given to the IDS submitted on May 5, 2004.

By this response, the specification has been amended to remove a reference numeral and claims 1 and 13 have been amended to clarify the subject matter defined in the claim. The amendments are believed to be proper and justified. No new matter has been added.

In view of both the amendments presented above and the following remarks, it is submitted that the claims pending in the application are novel and nonobvious. It is believed that this application is in condition for allowance. By this response, reconsideration of the present application is respectfully requested.

OBJECTION TO THE DRAWING

The drawings have been objected to for failing to include a reference sign mentioned in the description. Since the amendment to the specification above has deleted all reference signs to system 10, it is submitted that the drawings comply fully with 37 C.F.R. §1.84(p)(5). Accordingly, the grounds for this objection are believed to be obviated. Withdrawal of this objection is respectfully requested.

CITED ART

U.S. Patent 5,355,415 to Lee et al. ("*Lee*"), U.S. Patent 5,530,959 to Amrany ("*Amrany*"), Choi, D.W., "Parallel Scrambling Techniques for Digital Multiplexers", 1986 ("*Choi*"), and Kim et al., "Realizations of Parallel and Multibit-Parallel Shift Register Generators" ("*Kim*") are all cited and applied in the present Office Action.

CLAIMS REJECTIONS UUNDER35 USC §102

Claims 1-7 AND 13-16

Claims 1-7 and 13-16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lee. This rejection is respectfully traversed.

In the present Office Action on pages 4 and 5, the Examiner also referred to claims 9, 10, and 11 with respect to application of the Lee reference under 35 USC 102. But no prima facie case of anticipation was made out for the base independent claim for claims 9-11, namely, claim 8. Therefore, it is submitted that the references to these claims and the inclusion of them for this rejection was made in error. Further, it is submitted that these claims are not anticipated by Lee.

Claim 1, in part, calls for:

> *- digital logic means for determining an appropriate subset of said sequence of scramble bits based, at least in part on, a generator polynomial and one or more bits from a prior appropriate subset;*
> *- generating means for generating said appropriate subset based, at least in part on, said generator polynomial and said prior state wherein, for each bit of said set of data bits, at least one bit of said appropriate subset is associated therewith; and*
> *- digital operation means for performing a bitwise parallel digital operation between each bit of said set of data bits and said at least one bit of said appropriate subset associated therewith to produce an output set of data bits.*

Lee fails to teach, show, or suggest the determination and generation of the appropriate subset wherein, for each bit of the set of data bits, at least one bit of the appropriate subset is associated therewith. Lee also fails to teach, show, or suggest the digital operation means as defined in claim 1.

The Examiner has also included a reference to page 1053 of an IEEE article by Kim to support the rejection of the digital operation means. The reliance on this reference is misplaced. The article is not referenced in or incorporated into the Lee patent. In fact, the article appeared almost three full years after the Lee patent issued. That article cannot be used to establish the state of the art at the time of the Lee patent. Hence, the portion of the anticipation rejection based on this article is flawed and improper and should be withdrawn

In view of the reasons set forth above, it is submitted that claim 1 is not anticipated by Lee. It is therefore believed that claim 1 and the claims dependent

thereon, namely, claims 2-7, are allowable under 35 U.S.C. §102 and 35 U.S.C. §103. Withdrawal of this rejection is respectfully requested.

Claim 13 is a method claim that, in part, calls for:

> *c) generating said appropriate subset wherein, for each bit of said plurality of data bits, at least one bit of said appropriate subset is associated therewith;*
> *d) loading said appropriate subset in a storage means; and*
> *e) performing a bitwise parallel XOR operation between each bit of said plurality of data bits and said at least one bit of said appropriate subset associated therewith to produce an output set of data bits.*

Lee fails to teach, show, or suggest generating the appropriate subset wherein, for each bit of the plurality of data bits, at least one bit of the appropriate subset is associated therewith. Lee also fails to teach, show, or suggest performing a bitwise parallel XOR operation as completely defined in claim 13.

The Examiner has also included a reference to page 1058 of an IEEE article by Kim to support the rejection. As stated above, the reliance on this reference is misplaced. For all the reasons set forth above with respect to claim 1, it is submitted that the portion of the rejection based on this article is flawed and improper and should be withdrawn.

In view of the reasons set forth above, it is submitted that claim 13 is not anticipated by Lee. It is therefore believed that claim 13 and the claims dependent thereon, namely, claims 14-16 are allowable under 35 U.S.C. §102 and 35 U.S.C. §103. Withdrawal of this rejection is respectfully requested.

CLAIMS REJECTIONS UNDER 35 USC § 103

Claims 8-12

Claims 8-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Amrany. This rejection is respectfully traversed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all the claim limitations. *See MPEP § 2142.* Motivations to combine or modify

references must come from the references themselves or be within the body of knowledge in the art. *See MPEP § 2143.01.*

Lee has been discussed above. The Examiner has admitted that Lee fails to disclose a selector. Amrany was added in combination with Lee for the purpose of introducing the teachings of a selector. But the combination of Amrany with Lee still fails to teach, show, or suggest the limitations of claim 8.

In claim 8, the selection means is defined as, "selection means for selecting between a first set of data bits to be scrambled and a second set of data bits to be descrambled". In Amrany, the selector appears to be used to select between a scrambler input signal and an XOR output from the shift register on the scrambler side. Also in Amrany, a different selector appears to be to select between a descrambler input signal and an XOR output from the shift register on the descrambler side. At no point in the Amrany reference or in the Lee reference is there even a remote suggestion that a selector be used to choose between a set of data bits to be scrambled and another set of data bits to be descrambled. As a result, the combined references of Lee and Amrany fail to teach, show, or suggest all the elements of claim 8.

In light of the reasons set forth above, it is submitted that claim 8 would not have been obvious to a person of ordinary skill in the art upon a reading of Lee and Amrany, either separately or in combination. It is therefore believed that claim 8 and the claims dependent thereon, namely, claims 9-12 are allowable under 35 U.S.C. §103. Withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all the claims pending in this patent application are in condition for allowance. Reconsideration and allowance of all the claims are respectfully solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Gregory C. Ranieri, Esq. at (503) 439-6500 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

In the event there are any errors with respect to the fees for this response or any other papers related to this response, the Director is hereby given permission to charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3703.

Respectfully submitted,

Dated: **February 22, 2007**

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